

PCB 75026

7.1 Introduction

The purpose of the Gain Chain is to provide wideband amplification or attenuation over a large range of gains, controllable in 1 dB steps.

The required gain change is achieved by logic selection of a chain of amplifiers and attenuators.

7.1.1 Level, X-Talk, and Read Osc Functions

Gain is set indirectly by the front panel "dB COARSE" and "dB FINE" controls. These are read by the microcomputer which selects the appropriate gain settings.

7.1.2 THD and IMD Functions

The system 100% Level autoranges directly under microcomputer control, while the GAIN CHAIN is controlled automatically by the microcomputer in response to the signal level and the position of the "DISTORTION" range control.

7.1.3 Gain Control Model

The system is structured to optimise headroom, amplifier gain-bandwidth requirements and excess noise.

To understand the test set gain structure it is easiest to consider the GAIN CHAIN as a series of 7 attenuators followed by a fixed gain, as shown in Fig. 7.1.1 below.

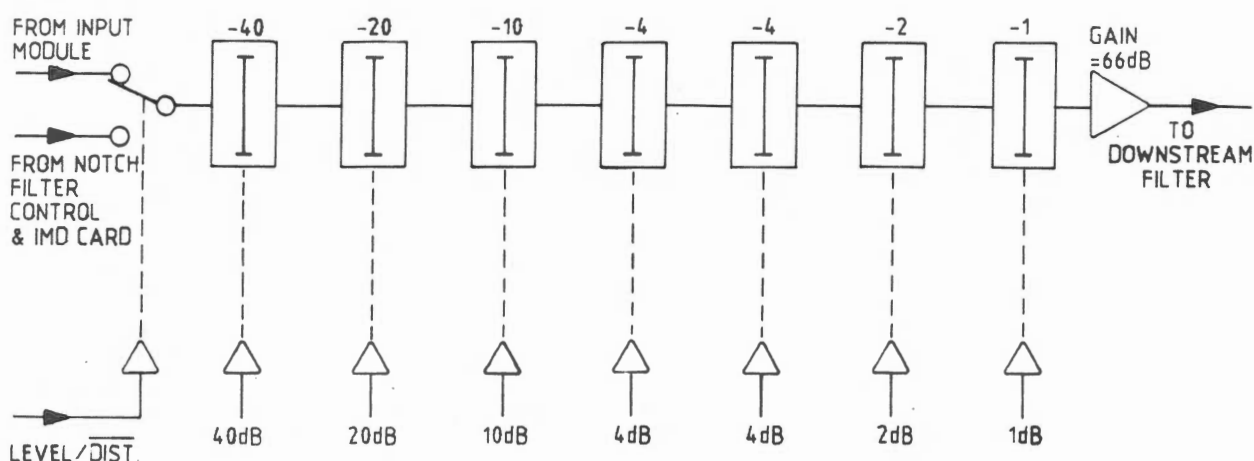


Figure 7.1.1 Simplified Gain Chain Model

When all of the control lines are LOW, the net gain is -15 dB. Raising each control line to the HIGH state adds the gain shown on the above drawing to the initial gain of -15 dB for the GAIN CHAIN system. Thus the gain is programmable in 1 dB steps from -15 dB to +66 dB.

7.1.4 Actual Circuit Model

In practice, the system gain is distributed as shown in Fig. 7.1.2 below, and the programmable gain amplifiers are used to provide part of the fixed gain as well as the variable gain. See Table 7.1.1 for control line status at the various test set gain settings.

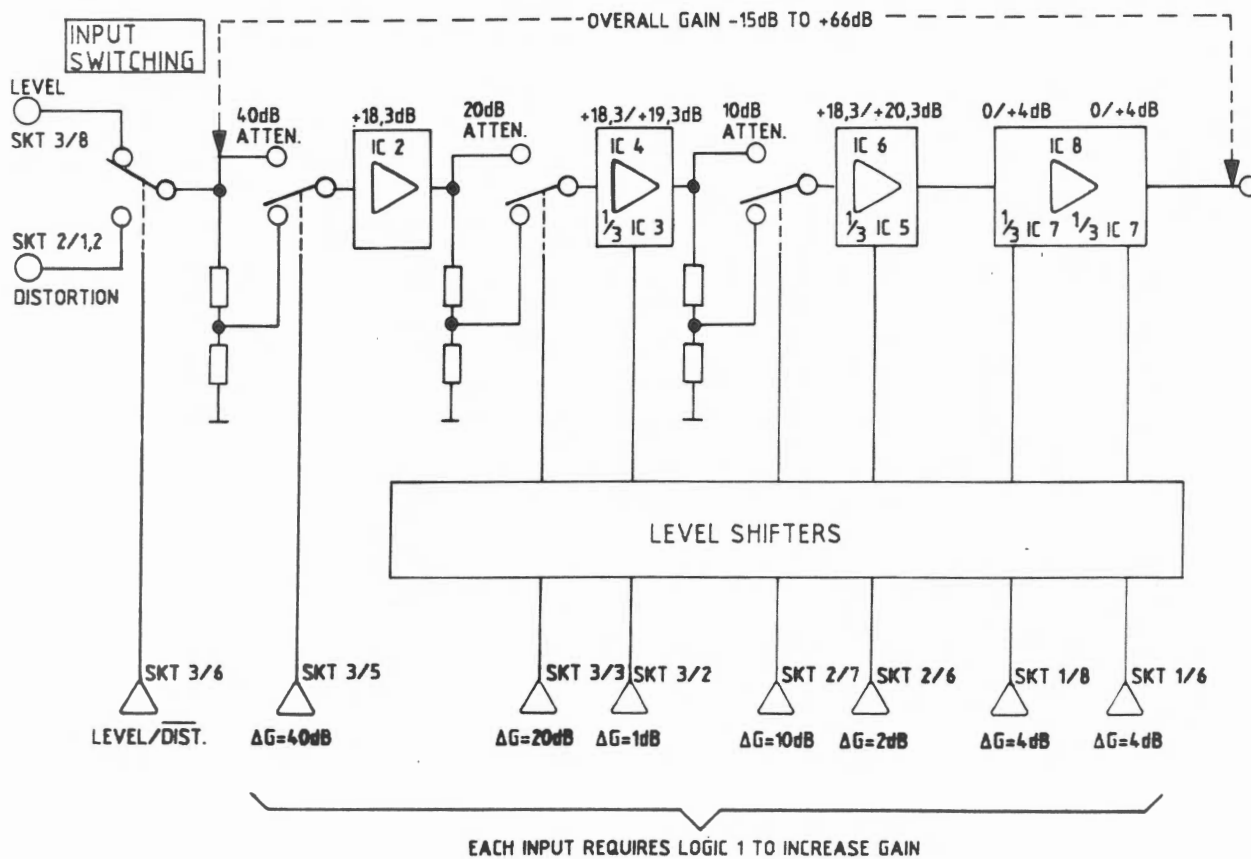


Figure 7.1.2 Gain Chain Block Diagram

		Gain Chain Section		
dB Coarse		-40 dB	-20 dB	10 dB
Input	+40 to -20	0	0	0
Setting	-30	0	0	1
	-40	0	1	0
	-50	0	1	1
	-60	1	0	0
	-70	1	0	1
	-80	1	1	0
	-90	1	1	1
Gain Chain Pin		SK 3/4	SK 3/2	SK 2/6
Microcomputer Pin		35	36	34

		Gain Chain Section			
dB Fine		+4 dB	+4 dB	+2 dB	+1 dB
Input	+5	0	0	0	0
Sensitivity	+4	0	0	0	1
Setting	+3	0	0	1	0
	+2	0	0	1	1
	+1	0	1	0	0
	0	0	1	0	1
	-1	0	1	1	0
	-2	0	1	1	1
	-3	1	1	0	0
	-4	1	1	0	1
	-5	1	1	1	0
Gain Chain pin		SK 1/8	SK 1/6	SK 2/6	SK 3/2
Microcomputer pin		32	29	31	33

TABLE 7.1.1 Gain Chain Operation - LEVEL/X-TALK/READ OSC Functions

7.2 Circuit Description

7.2.1 Input Selector

The input signal to the gain chain is selected according to the measuring function. It can be derived either directly from the input amplifier output (LEVEL, X-TALK, READ OSC), via SK3/8 and C1, or from the notch filter output (THD+N) or the IMD system (IMD) via SK2/1&2 and C2. A logic input to the driver of an analogue switch (part of IC1) selects the appropriate input.

A logic 1 (HIGH) selects the "LEVEL" input; a logic 0 (LOW) selects the "IMD/THD" input.

When "LEVEL" is selected (logic 1 on SK3/6), switch IC1/16,1 is closed and IC1/4,3 is open. The input via C1 is routed to the 40 dB attenuator.

When "THD" or "IMD" is selected (logic 0 on SK3/6), the condition shown on the circuit diagram is valid; namely, switch IC1/4,3 is closed and IC1/16,1 is open. The input via C2 is routed to the 40 dB attenuator.

7.2.2 40 dB Attenuator

The selected input signal is applied to IC1/9 at the top end of R10, the series arm of the 40 dB attenuator.

In the low gain condition, the signal is switched via IC1/5,6 to the non-inverting input of IC2, with switch IC1/9,8 open, as shown. In this condition, the 40 dB attenuator formed by series arm R10, and shunt arm R9//VR1 and R11 is in circuit.

A logic 1 (HIGH) on SK3/5 is applied to the driver via IC1/10. This results in the signal now being switched via IC1/9,8, to the non-inverting input of IC2, with IC1/5,6 open, removing the 40 dB attenuator from the circuit.

VR1 trims the gain change to exactly 40 dB.

7.2.3 18.3 dB Gain Amplifier

Amplifier IC2 is one of three similar operational amplifiers, (IC2, IC4 and IC6), each with a gain of 18.3 dB to give an overall gain of 55 dB over the three stages.

Feedback to the inverting input IC2/2 is via resistor R20, to give a stage gain of:

$$\frac{R20 + R17}{R17} = 8.273 \times = 18.35 \text{ dB}$$

The output on IC2/6 is applied via C8 to the 20 dB attenuator.

7.2.4 20 dB Attenuator

In the -20 dB gain state (logic 0 on SK3/3) the 20 dB attenuator is in circuit.

Transistor TR1 acts as an inverting level shifter to accommodate the CMOS

logic of the analogue switches of IC3. The logic 0 on the base of TR1 gives a logic 1 at the collector. The logic 1 on driver inputs IC3/10 and IC3/11 means that the signal paths are: IC3/15,1 and IC3/14,13. The attenuator consists of the series arm, R24; and the shunt arm, $R21/(VR2 + R25)$. IC3/15,1 serves to shunt the signal on pin 15 to earth, thus preventing any capacitive coupling of the signal via IC3/15,2 in the off state.

A logic 1 on SK3/3 produces a logic 0 on the collector of TR1 which is applied to driver inputs IC3/10 and IC3/11. This results in switching the signal via IC3/15,2 and IC3/14,12. The signal into the attenuator shunt arm is short-circuited by IC3/14,12. Thus an unattenuated signal is applied to IC4.

VR2 is used to adjust the gain change to exactly 20 dB.

7.2.5 18.3/19.3 dB Amplifier

Amplifier IC4 is a non-inverting operational amplifier stage with feedback set by R30 and R31 to give a gain of 18.35 dB. This gain can be increased by 1 dB when a logic 1 (HIGH) signal is applied to SK3/2.

7.2.6 18.3 dB Gain State

This is the state with a logic 0 on SK3/2, producing a logic 1 on the collector of the inverting level shifter TR2 which is applied to IC3/9. Resistor R28 is short-circuited by IC3/4,3.

The gain is given by $\frac{R31 + R30}{R31} = 8.273 \times$ (18.35 dB)

7.2.7 19.3 dB Gain State

In this state a logic 1 on SK3/2 produces a logic 0 on TR2 collector to IC3/9. Switch IC3/4,3 opens to remove the short-circuit across R28. This resistor is then connected in parallel with R31 by the switch IC3/4,5. This reduction in resistance from the inverting input to earth gives a gain increase of 1 dB.

7.2.8 10 dB Attenuator

The 10 dB attenuator is formed from R34, R37 and R35, with VR4 to trim the attenuation to exactly 10 dB. IC5 switches between the two gain states, and TR3 functions as a level shifter to drive the relevant sections of IC5.

7.2.9 -10 dB Gain State

In this state a logic 0 is placed on SK2/7 and the 10 dB attenuator is in circuit.

The level shifter TR3 inverts the logic 0 applied to its base to give a logic 1 on the switch inputs IC5/10 and IC5/11.

The signal paths are switch IC5/15,1 and switch IC5/14,13. The attenuator consists of the series arm, R34, and the shunt arm, $R37/(VR4 + R35)$. The switch IC5/15,1 serves to shunt the signal on pin 15 to earth to prevent unwanted capacitive coupling.

VR4 trims the attenuation to exactly 10 dB.

7.2.10 0 dB Gain State

In this state a logic 1 is placed on SK2/7. A logic 0 is applied (via TR2) to inputs IC5/10 and IC5/11.

The signal is routed without attenuation through switch IC5/15,2 to the non-inverting input of IC6, and R34 is connected to earth via IC5/14,12; i.e. the shunt arm of the attenuator is short-circuited.

Switches IC5/15,1 and IC5/14,13 are open.

7.2.11 18.3/20.3 dB Amplifier

Amplifier IC6 is a non-inverting op-amp with feedback via R44 and R42 to give a gain of 18.35 dB. This gain can be increased by 2 dB when a logic 1 (HIGH) signal is applied to SK2/6.

7.2.12 18.3 dB Gain State

In this state a logic 0 is placed on SK2/6.

A logic 1 on the collector of inverting level shifter TR4 is applied to driver input IC5/9. The feedback is via voltage divider R44 and R45 through a series resistance consisting of R41//R42, since switch IC5/4,3 is closed (IC5/4,5 open).

7.2.13 20.3 dB Gain State

In this state a logic 1 is placed on SK2/6.

A logic 0 is applied via TR4 to driver input IC5/9. Switch IC5/4,3 opens and R41 and the small resistor R42 are switched across R45 by switch IC5/4,5.

This reduction in feedback factor gives a gain change of +2 dB.

7.2.14 0/+4/+8 dB Amplifier

Amplifier IC8 is an inverting op-amp with gain set by R53/R50 to give a gain of 1.519x (+3.96 dB). The gain can be reduced by 4 dB by switching in more feedback via R55 and R56, or can be increased by 4 dB by switching in R48 and R54 in the forward path.

7.2.15 0 dB Gain State

The input resistance consists of R50. With SK1/8 input at logic 0, a logic 1 on the collector of the level shifter inverter TR5 is applied to driver input IC7/9 to shunt the signal at the R48, R54 junction to earth via switch IC7/4,3.

Switch IC7/4,5 is open.

With SK1/6 input at logic 0, a logic 1 on the collector of the level shifter inverter TR6 is applied to driver input IC7/10.

The switch IC7/1,15 connects the network consisting of R56, VR7 and R55 across

the feedback resistor R53 to give a gain of approximately 0 dB. VR7 trims the gain change to exactly 4.00 dB.

7.2.16 +4 dB Gain State - Stage 1

With SK1/8 input at logic 1, a logic 0 (via TR5) is applied to driver input IC7/9. Switch IC7/4,3 opens to disconnect the junction of R54, R48 from earth and connects this point to the inverting input of IC8, effectively reducing the input resistance presented by R50. SK1/6 input remains at Logic 0.

7.2.17 +4 db Gain State - Stage 2

With SK1/6 input at logic 1, a logic 0 (via TR6) is applied to driver input IC7/10. Switch IC7/1,15 opens and disconnects R55/R56 network from the feedback path and switch IC7/15,2 connects R56 to earth.

VR7 trims the gain change to exactly 4 dB.

The Gain Chain output on IC8/6 is applied via edge connector SK1/3 to the filters.

7.2.18 ±18V Supplies

The Gain Chain board is supplied from the +18 V rail (SK2/4) and the -18 V rail (SK2/5). These supply IC1, IC2, IC4, IC6 and IC8. IC2 has its rails separately decoupled by R18/C6 and R19/C7.

7.2.19 +5 V Supplies

IC1 is supplied at pin 12 with a +5 V supply derived from the +18 V rail via potential divider R12, R14 and decoupled by C5.

7.2.20 ±8.1 V Supplies

The +8.1 V and -8.1 V supplies for IC3, IC5 and IC7 (CMOS 4053 ICs) are derived from the +18 V and -18 V rails respectively.

The +18 V supply is dropped via R3 to give +8.1 V shunt regulated by D1 and Zener diode D2 in series and decoupled by C3.

In an identical circuit, the -18 V supply is dropped via R4, D3 and D4 to give -8.1 V.

7.2.21 ±7.5 V Supplies

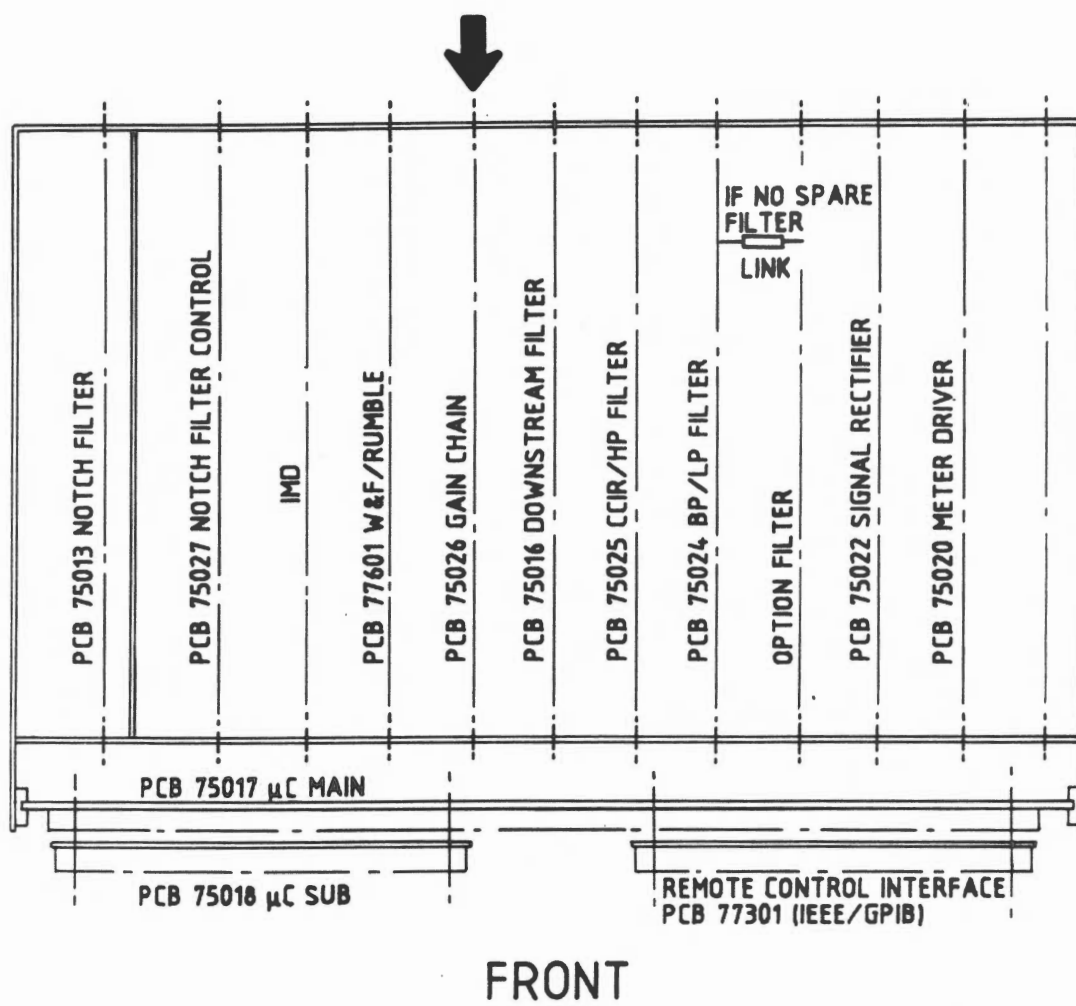
The +7.5 V and -7.5 V supplies across the Zener diodes D2 and D3 are used with clamping diodes D5, D6, and D7, D8 and R26, R36 to ensure that large signal excursions cannot unintentionally turn on the CMOS switching ICs by exceeding the ±8.1 V supplies.

7.3 Removal/Replacement

Switch off the MJS401D and remove the mains lead.

Remove the four screws retaining the top cover. Pull the top cover straight up.

With the instrument facing you, the GAIN CHAIN card is installed in the 5th slot from the left in the main card frame. Verify by noting the printing on the motherboard.



MJS401D PCB Location Guide

Remove the card by grasping the top corners and gently pulling up.

Replacement is the opposite of removal. Carefully line up the connectors before pushing down and ensure the card is properly held within the guides.

Extender card PCB75033 may be used to facilitate repair and calibration.

7.4 Fault Finding

7.4.1 General

Use extender card PCB 75033.

The extender card contains a number of LEDs and test points to aid the repair and calibration process. The following procedure uses these frequently to guide fault tracing.

The most likely faults in the GAIN CHAIN are easily traced to the appropriate stage by use of the chart below. This method allows each stage of the card to be activated independently. A signal applied to the extender card GAIN CHAIN I/P test point and measured at the GAIN CHAIN O/P provides a quick guide to a failed switch or signal path.

The signal can then be examined directly at the input and output of the stage in question.

7.4.2 D.C. Checks

Check all the points shown on the circuit drawing to ensure correct D.C. operation.

7.4.3 Main Functional Checks

MJS401D Front Panel Setup

Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	Level	Off	AVG	dB Norm	---	-20	+5

Check Extender LED "LEVEL" in ON. SKT3/6 High (+5 V)
 Extender LED "DIST" is OFF.

If these are incorrect, check microcomputer pin 39 is high.

If pin 39 is low, confirm LEVEL LED is ON on front panel. If so either there is a short on the line or IC34 is likely to be faulty on the microcomputer.

If SKT3/6 is low, but pin 39 high - fault most likely in motherboard or interconnects between it and the microcomputer or Gain Chain PCB.

7.4.4 Gain Stage Checks

Connect a sinewave oscillator to the MJS401D Input

Source Level: -20 dBu (0.0775 V)

Check Meter Reading = -5 NOTE if different

Whether the meter is correct or not, proceed through the following checks.
Note CHANGES in the meter level display.

SOURCE LEVEL	<u>SENSITIVITY SETTINGS</u>		EXTENDER LED ON	GAIN CHAIN CONTROL PIN	uCOMP PIN	GAIN CHAIN SECTION
	dB COARSE	dB FINE				
-20 dB		+5	-	-	-	Min Gain
-21 dB	-20	+4	1dB	SK3/2	33	18.3/19.3 Gain Amp
-22 dB	-20	+3	2dB	SK2/6	31	18.3/20.3 Gain Amp
-24 dB	-20	+1	4dB	SK1/6	29	+4 (stage 2)
-28 dB	-20	-3	4dB,4dB	SK1/6 & SK1/8	29,32	Both +4 stages
-30 dB	-30	+5	10dB	SK2/7	34	10 dB ATTN
-40 dB	-40	+5	20dB	SK3/3	36	20 dB ATTN
-60 dB	-60	+5	40dB	SK3/5	35	40 dB ATTN

Appreciable meter level changes indicate a fault. If the extender LEDs indicate the correct gain, the fault is in the Gain Chain. If not, the SWITCHES or ENCODERS (Section 12) or MICROCOMPUTER SYSTEM (Section 3) or MOTHERBOARD AND INTERCONNECTION (Section 2) are suspect.

7.4.5 Function Checks

Function	Extender LED	SK3/6 status
LEVEL	LEVEL	+5 V
X-TALK	LEVEL	+5 V
READ-OSC	LEVEL	+5 V
THD + N	DIST	0 V
IMD (if fitted)	DIST	0 V

7.5 Calibration

Use Extender Card PCB 75033.

7.5.1 General

For accurate calibration a precision calibrated AC DVM with adequate bandwidth is required together with a stable sinewave oscillator. If the DVM has not been calibrated within the last 6 months, have it calibrated by a laboratory with traceable standards before using it to calibrate the MJS401D.

Recommended specifications:-

DVM 4.5 digit
 1 kHz minimum bandwidth

OSC Frequency approx. 400 Hz
 < 1% distortion
 Level stability < ± 0.05 dB over 30 minutes
 Output level controllable over a range greater than 40 dB without serious degradation of signal-to-noise ratio

7.5.2 D.C. Adjustments

Check D.C. conditions:

D2	cathode	+7.2 V	to	+7.9 V
D3	anode	-7.2 V	to	-7.9 V
D1	anode	+7.8 V	to	+8.5 V
D4	cathode	-7.8 V	to	-8.5 V
IC1	pin 12	+4.8 V	to	+5.2 V
IC2	pin 4	-17.3 V	to	-17.7 V
IC2	pin 7	+17.3 V	to	+17.7 V
IC8	pin 6	+12 mV	to	-12 mV

Measure the voltage between IC4/6 and GROUND. Adjust VR3 to set this to 0 V.

Measure the voltage between IC6/6 and GROUND. Adjust VR5 to set this to 0 V.

7.5.3 Gain Calibration

MJS401D Front Panel Setup

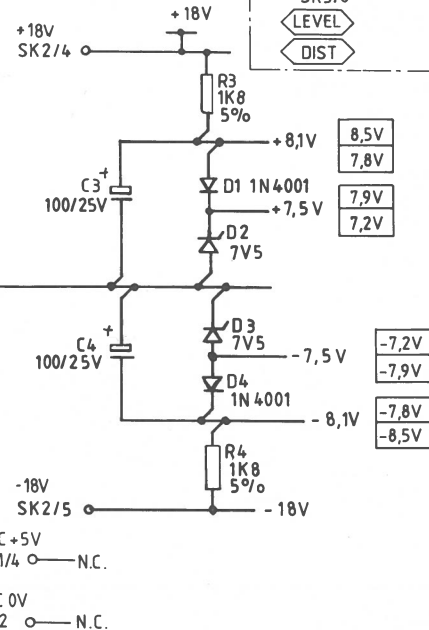
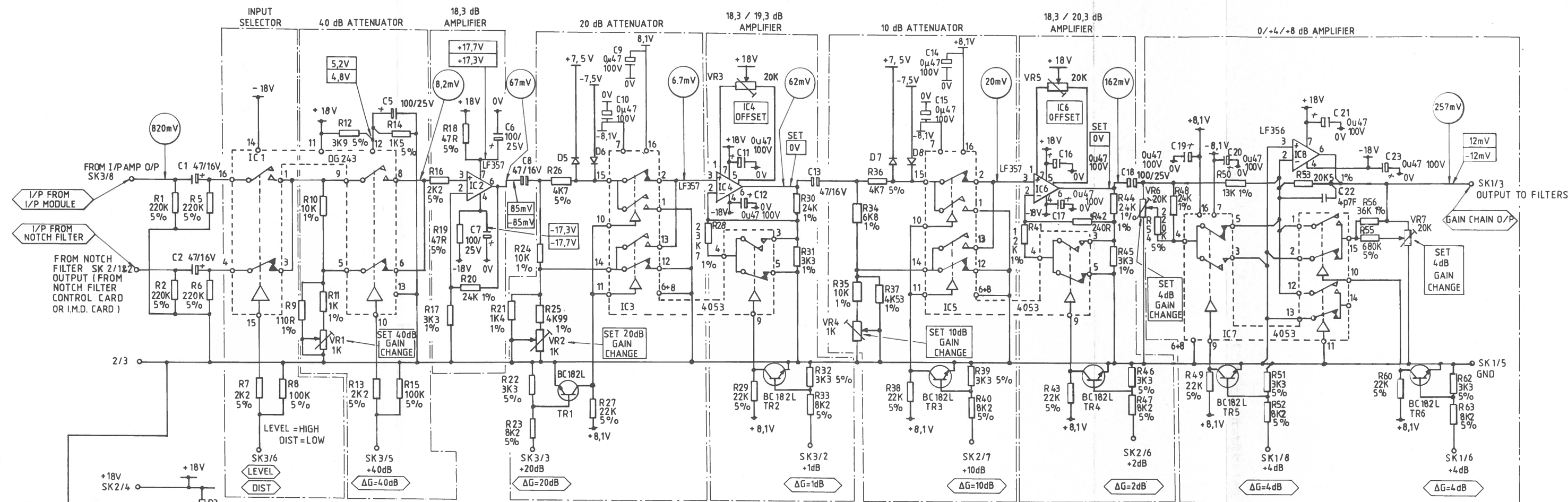
Input	Load	Function	Filters	Rectifier	Scale	Dist'n	Coarse	Fine
A	Off	Level	30k	RMS	dB Exp	---	-30	0

Connect DVM to GAIN CHAIN O/P test point. Ensure that the extra capacitive loading does not cause the gain chain to oscillate.

Connect source to Input A via an attenuator. The attenuation should be such that a level of -21 dBu emerges from the attenuator when the source is operating near its maximum output level. The DVM will need to be connected to the source side of this attenuator on two occasions during this calibration procedure. Set the source frequency to approx. 400 Hz.

ADJUST	FRONT PANEL SENSITIVITY SETTINGS		DVM READING		PURPOSE
	dB COARSE	dB FINE	VOLTS	dBu	
SOURCE	-30	+1	2.451 V	(+10 dBu)	Ref level
VR4	-20	+1	0.7750 V	(0 dBu)	Set 10 dB gain step
Check only	-20	0	0.8696 V	(+1 dBu)	Check 1 dB gain step
Check only	-20	-1	0.9757 V	(+2 dBu)	Check 2 dB gain step
VR7 (stage 2)	-20	+5	0.4890 V	(-4 dBu)	Set 4 dB gain step
VR6 (stage 1)	-20	-3	1.2283 V	(+4 dBu)	Set 4 dB gain step
SOURCE	-40	+1	0.7750 V	(0 dBu)	Ref level
Connect DVM to source. Note reading. Increase by EXACTLY a factor of 10. Reconnect DVM to GAIN CHAIN O/P test point.					
VR2	-20	+1	0.7750 V	(0 dBu)	Set 20dB gain step
SOURCE	-60	+1	0.7750 V	(0 dBu)	Ref Level
Connect DVM to source. Note reading. Increase by EXACTLY a factor of 100. Reconnect DVM to GAIN CHAIN O/P test point.					
VR1	-20	+1	0.7750 V	(0 dBu)	Set 40 dB gain step

REVISION			
NO	DATE	CHANGE	APPROVED
3	6-3-84	R54 REISSUED. R55, 56 VALUES CHANGED. VR6, 7 ADDED. R42 VALUE CHANGED. C18 CHANGED.	



D5 TO D8 = 1N 4148

REPRESENTS A.C. VOLTAGES MEASURED WITH AN INPUT IMPEDANCE OF 10K OHMS OR GREATER. UNLESS OTHERWISE SPECIFIED THESE LEVELS CORRESPOND TO A 1KHz TONE AT A REFERENCE LEVEL OF 0dBu (0.775V) INTO A FULLY CALIBRATED TEST SET, 'LEVEL' FUNCTION, 0dB RANGE.

REPRESENTS D.C. VOLTAGES MEASURED WITH A VOLT-METER OF 20,000Ω/V OR GREATER. MAXIMUM IS DEFINED AS THE MOST POSITIVE VOLTAGE.

USE EXTENDER CARD PCB 75033

EXTENDER TEST POINT OR INDICATOR REFERENCE

HIGHEST	MISSING
R63	R57,58,59,61
C23	-
VR7	-
TR6	-
D8	-
IC8	-

NEUTRIK AG Unit 2, Samuel Whites Industrial Estate, Medina Road, Cowes, Isle of Wight, PO31 7LP, GB Tel: (0983) 299959 Telefax: (0983) 290142		TITLE GAIN CHAIN	
		USE 401D TEST SET	
TOLERANCES - UNLESS OTHERWISE STATED Linear Millimetres ±0.4mm Angular Degrees ±0.25°		DRAWING NO	
MATERIAL		DATE 10/3/83	
FINISH		PROJECT NO 750	
		TYPE C	
		SHEET NO 076	
		SIZE 1	
		REV 3	